CLAIMS

What is claimed is:

1. An apparatus, comprising:

an integrated circuit having:

N queues to receive commands for a memory device, the memory device having M banks, the N queues having a first queue and a second queue to map to a first bank; and

logic to:

determine a last type of command de-queued,

determine a bank designated to receive a next command to be de-queued,

inspect the first and the second queues for a type of command matching the last type of command de-queued,

de-queue the command that matches the last type of command de-queued, and

send the de-queued command to the designated bank.

2. The apparatus of claim 1, wherein the designated bank is the next sequential bank.

3. The apparatus of claim 1, wherein the N queues further include:

a third queue and a fourth queue to map to a second bank;

a fifth queue and a sixth queue to map to a third bank; and

a seventh queue and an eighth queue to map to a fourth bank.

4. The apparatus of claim 3, wherein the memory device is located in a memory module having a first side and a second side, and wherein the first queue, the second queue, the third queue, and the fourth queue map to the first side.

5. The apparatus of claim 4, wherein the fifth queue, the sixth queue, the seventh queue, and the eighth queue map to the second side.

6. An article of manufacture, comprising a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving commands in N queues for a memory device, the memory device having M banks, the N queues having a first queue and a second queue to map to a first bank; and

determining a last type of command de-queued;

determining a bank designated to receive a next command to be de-queued;

inspecting first and second queues for a type of command matching the last type of command de-queued;

de-queuing the command that matches the last type of command de-queued; and

sending the de-queued command to the designated bank.

7. The article of manufacture of claim 6, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising determining a last bank to receive a command and sending the de-queued command to a next sequential bank.

8. The article of manufacture of claim 6, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising:

mapping a third queue and a fourth queue to a second bank;

mapping a fifth queue and a sixth queue to a third bank; and

mapping a seventh queue and an eighth queue to a fourth bank.

9. The article of manufacture of claim of claim 8, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising mapping the first queue, the second queue, the third

queue, and the fourth queue map to a first side of a memory module on which the memory device is located.

10. The article of manufacture of claim of claim 9, mapping the fifth queue, the sixth queue, the seventh queue, and the eighth queue to a second side of the memory module.

11. A system, comprising:

an integrated circuit having:

N queues to receive commands for a memory device, the memory device having M banks, the N queues having a first queue and a second queue to map to a first bank; and

logic to determine a last type of command de-queued, determine a bank designated to receive a next command to be de-queued, inspect the first and the second queues for a type of command matching the last type of command de-queued, de-queue the command that matches the last type of command de-queued, and send the de-queued command to the designated bank; and

a dual in-line memory module (DIMM) having the designated bank, the memory module to receive the de-queued command.

12. The system of claim 11, wherein the dual in-line memory module (DIMM) is a single-sided memory module.

13. The system of claim 11, wherein the dual in-line memory module (DIMM) is a multiple-sided memory module.

14. An apparatus, comprising:

an integrated circuit having:

N queues to receive commands for a memory device, the memory device having M banks, the N queues having a first queue and a second queue to map to a first bank; and

logic to:

determine a last type of command de-queued,

determine a bank designated to receive a next command to be de-queued, wherein the designated bank is the next sequential bank after a bank to receive a last de-queued command,

inspect the first and the second queues for a type of command matching the last type of command de-queued,

de-queue the command that matches the last type of command de-queued, and

send the de-queued command to the designated bank.

15. The apparatus of claim 14, wherein the N queues further include:

a third queue and a fourth queue to map to a second bank;

a fifth queue and a sixth queue to map to a third bank; and

a seventh queue and an eighth queue to map to a fourth bank.

16. The apparatus of claim 15, wherein the memory device is located in a memory module having a first side and a second side, and wherein the first queue, the second queue, the third queue, and the fourth queue map to the first side.

17. The apparatus of claim 16, wherein the fifth queue, the sixth queue, the seventh queue, and the eighth queue map to the second side.

18. The apparatus of claim 14, wherein the integrated circuit further includes logic to determine that the memory device includes four banks.

19. The apparatus of claim 14, wherein the integrated circuit further includes logic to determine that the memory device includes eight banks.

20. The apparatus of claim 14, wherein the integrated circuit further includes logic to determine that the memory module includes one side.

21. The apparatus of claim 14, wherein the integrated circuit further includes logic to determine that the memory module includes two sides.